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10/083,351	02/27/2002	Noboru Hosokawa	500.41299X00	5746

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MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
NGUYEN BA, HOANG VU A	
ART UNIT	**PAPER NUMBER**
2623	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,351	HOSOKAWA, NOBORU	
	Examiner	Art Unit	
	Hoang-Vu A. Nguyen-Ba	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed May 4, 2007.

2. Claims 1-9 remain pending. Claim 1 is an independent claim.

Response to Amendments

3. Per Applicant's request, Claims 1, 6 and 7 have been amended.

Response to Argument

4. Applicant's arguments in the Remarks, filed concurrently with the Amendment, have been fully considered but are not persuasive. Following is an examiner's response to Applicant's arguments.

a. Applicant essentially argues that the conventional apparatus, such as that taught in the Background of the Invention section of the present application, provides for a plurality of dedicated buses which in effect connect the various elements including the JPEG compression circuit, network control circuit and storage unit in parallel to the CPU, accomplishing the simultaneous and independent operation discussed therein and therefore, the Background of the Invention section of the present application teaches a conventional apparatus which provides for a parallel connection of the various elements rather than a series connection as now more clearly recited in the claims.

In response to the above argument, the examiner respectfully notes the following definition of a bus By Microsoft® Technet:

A data pathway that connects the different parts of a computer memory, processor, disk drives, and so on. The bus consists of multiple conducting wires (lines) running in parallel. Different lines are used to carry different types of information, including memory locations, data,

and control signals.
www.microsoft.com/technet/prodtechnol/visio/visio2002/plan/glossary.mspx

The amended claims recite *a first bus for providing a series connection* (which is as an initial matter merely an alternative recitation of the same limitation -- i.e., a first bus for connecting in series -- previously recited in the original claims; therefore, the amended claims do not help clearly distinguish over the APA). In view of the definition of a bus provided by Microsoft®, the claimed *first bus* can be interpreted to be a data pathway that connects different parts of a circuit (which can be disposed physically on the circuit board one after another) and that consists of multiple conducting wires running in parallel (e.g., the wire or a series of wire running in parallel – bus—that enables CPU to simultaneously and independently exchange data with the JPEG compression circuit can coexist **side-by-side or in parallel** with a wire or a bus of wires that enables CPU gains access to data for an execution command of CPU itself and for data to be processed inside the claimed *first bus* notwithstanding the fact that the CPU may be located before or after the JPEG compression circuit along the *first bus* data path).

Therefore, the amended claims still read on the APA of the Background of Applicant's disclosure.

b. Applicant further argued that APA fails to teach or suggest that the first bus and the second bus are connected through a first bus buffer as claimed.

In response to this argument, it is noted that the added limitation bus does not help the amended claims distinguish over the APA teachings because the function of buffering remains the same whether

the component that performs the buffering function is a bus or other type of component.

In view of the foregoing discussion, the rejections of claims 1-9 are maintained and repeated hereinafter for Applicant's convenience.

Claim Rejections – 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejection under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 and 7 are rejected under 35 U.S.C. § 102(b) as being anticipated by the admitted prior art (APA) of pages 1-3 of Applicant's background.

Claim 1

APA discloses at least:

a central processing unit block (p. 2, lines 1-2)*; and*

a peripheral block, wherein said peripheral block includes a video processing unit for processing video signals from an image picking-up device and generating video data, a network control unit for controlling transmission and reception of said video data transmitted and received through a transmission medium inclusive of a network (see at least p.1, lines 7-22), *and a first bus for providing a ~~connecting in series~~*

series connection without any branch of said video processing unit and said network control unit (see at least p.2, line 27 to p. 3, line 7);

wherein said central processing unit block includes a central processing unit for processing said video data, a storage unit for storing video data from said video processing unit, a central control unit for controlling said video processing unit, said network control unit and said storage unit in cooperation with said central processing unit, and a second bus for providing a ~~connecting in series~~ series connection of said central processing unit, said storage unit and said central control unit (p. 2, line 2 to p. 3, line 7), *and*

wherein said first bus and said second bus are connected through a first bus buffer (see at least p. 3, lines 8-15).

Claim 2

APA further discloses *wherein said central processing unit and said central control unit control said video processing unit, process the video signals from said image picking-up device and store the compressed video signals in a cycle of 1/30 fps and at a data transmission rate of at least 3.6 Mbps in said storage unit through said first bus, said first bus buffer and said second bus* (see at least p. 2, lines 2-16; it is noted that storing data at a rate of 1/30 fps and transmitting data at a rate of 3.6 Mbps through the bus appear to be admitted by Applicants as known in the art since Applicants claim in their disclosure that their system can transmit twice as fast as 3.6 Mbps (i.e., 7.2 Mbps at p. 9, line 21).

Claim 3

APA does not specifically disclose *wherein said central processing unit and said control unit read out said compressed video data from said storage unit at a data transmission*

rate of at least 14.4 Mbps for a request of four users from said network control unit, and transmit said compressed video data to said network control unit through said second bus, said first bus buffer and said first bus. However, this feature is deemed inherent to APA because of the following reasons:

APA discloses at p. 3, lines 8-15 that using a plurality of DMA transmission functions for executing data access with a built-in buffer and with external equipment independently of command execution of CPU itself and a plurality of interfaces for exchanging data by using the DMA transmission functions under the state where no processing load is applied to CPU itself; and

since the read out function is not *per se* one that requires the processing of the CPU

a simultaneous request of 4 users (3.6 Mbps/each * 4 = 14.4 Mbps) requiring 14.4 Mbps is deemed inherent to the circuit design incorporating a plurality of DAM transmission functions (e.g., 4 buffers).

Claim 7

APA does not specifically disclose *wherein said first bus further ~~connects in~~ provides a series connection of a circuit for displaying an operating condition of said video transmission apparatus and a switch circuit for setting an operation of said video transmission apparatus.* However, these features are deemed inherent to APA because as discussed at p. 3, lines 16-27 of Applicant's background: 1) a CPU can connect to a JPEG compression circuit **or** a network control circuit; and 2) the aforementioned connection can be implemented through an interface; it is understood that there must be provided a switch in order to select either the JPEG compression circuit or the network control circuit and thus the switching

function could be shown via the interface as to which connection is under operation. Without these inherent features, the system is inoperative.

Claim Rejections – 35 USC § 103

7. The following is a quotation of the 35 U.S.C. § 103(a) which form the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not negatived by the manner in which the invention was made.

8. Claims 4-6 and 8-9 are rejected under 35 U.S.C. § 103(a) as being obvious over the admitted prior art of pages 2-5 of Applicant's background.

Claim 4

APA does not specifically disclose *wherein a second bus buffer is further connected in series to said second bus, and a third bus having expansion connectors connected thereto is connected to said second bus buffer.* However, APA does disclose that recent CPU has a plurality of DMA transmission functions for executing data access with a built-in buffer and with external equipment independently of command execution of CPU itself and a plurality of interfaces for exchanging data by using the DMA transmission functions. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use this capability for transmitting data independently of command execution of CPU, as this would reduce overhead and increase the speed of transmission.

Claim 5

APA does not specifically disclose *wherein a video expansion unit is connected in series to said expansion connectors of said third bus, and a monitor is connected to said video expansion unit.* However, APA does disclose that recent CPU has a plurality of DMA transmission functions for executing data access with a built-in buffer and with external equipment independently of command execution of CPU itself and a plurality of interfaces for exchanging data by using the DMA transmission functions. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use this capability for transmitting data independently of command execution of CPU, as this would reduce overhead and increase the speed of transmission.

Claim 6

APA does not specifically disclose *wherein said second bus provided to said central processing block unit connects said central processing unit, said storage unit, said central control unit and said first bus buffer in order named, and said first bus provided to said peripheral block connects said first bus buffer, said network control unit and said video processing unit in order named.* However, APA does disclose that in order to conduct data transmission operations at a high speed, some video apparatuses employ a plurality of dedicated bus systems and that such systems enable CPU to simultaneously and independently exchange data with the JPEG compression circuit and with the network control circuit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify such a system such that these dedicated bus could be named in order. One of ordinary skill in the art would have been motivated to do so for

the purpose of facilitating the installation and the troubleshooting of additional dedicated bus systems.

Claim 8

APA does not specifically disclose *wherein a dumping resistor is connected to a starting point or an end point of each of said first and second buses and a terminating resistor is connected to the other.* However, Official notice is taken that dumping resistor is well known in the art to be used for the purpose of matching the characteristic impedance of two circuits on a wiring board and terminating resistor is well known in the art to be used in wiring board for the purpose of minimizing the deterioration of signal qualities without changing the constitution of a semi-conductor unit (e.g., Abstract of JP 2002124775 A).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use dumping and terminating resistors in APA when connecting additional bus for the purposes discussed above.

Claim 9

APA does not specifically disclose *wherein said peripheral block and said central processing unit block are arranged on the same packaging board, said central processing unit and said central control unit are positioned at said central processing unit block which is located at a substantial center of said packaging board, and said peripheral block is disposed at a peripheral area of said central processing unit block of said packaging board.* However, the positioning of the CPU and control unit at the center of circuit board is considered to be a matter of design choice for the purpose of providing the circuit with expansion capability by leaving the outer layer of the circuit board available for connection with add-on circuits and by minimizing

the distance from the CPU and control unit to theses add-on circuits by the virtue of the CPU and control unit being at the center location on the circuit board.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the aforementioned design choice in the list of choices available in APA for the purposes discussed above.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu "Antony" Nguyen-Ba whose telephone number is (571) 272-3701. The examiner can normally be reached on Tuesday-Friday from 7:00 am to 5:30 pm.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, John Miller can be reached at (571) 272-7353.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2600 Group receptionist (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

July 22, 2007

ANTONY NGUYEN-BA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100